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EXAMINER	
GU, SHAWN X	

ART UNIT	PAPER NUMBER
2189	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/821,549	PERI ET AL.	
	Examiner	Art Unit	
	Shawn X. Gu	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 June 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17 and 34-45* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-8 and 40-45* is/are allowed.

6)☒ Claim(s) *9-17 and 34-38* is/are rejected.

7)☒ Claim(s) *39* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This final Office action is in response to the amendment filed 31 May 2007. Claims 1, 2, 4-17 and 34-45 are pending. Claims 3 and 18-33 are cancelled. All objections and rejections not repeated below are withdrawn.

Claim Objections

2. Claim 39 is objected to because of the following informalities:

On line 2, "is invalid" should be replaced by "are invalid".

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 9-17 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Per claim 9, the limitation "the plurality of buffers are present within the cache memory" is not supported by the Applicant's disclosure. Figures 4 and 8 clearly show that the buffers are outside of the cache memory, and no part of the specification discloses the buffers are within the cache memory. Moreover, having the buffers within the cache memory seems to contradict to features of Applicant's claimed invention, since the invention aims to use the buffers as a faster cache than a L1 cache in order to reduce access latency. If the buffers are within the cache memory then latency will not be reduced.

All dependent claims are rejected to for having the same deficiencies contained in the claims they are dependent from. Appropriate correction is required.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 13-17 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Per claim 13, the limitation "the load buffers" lack sufficient antecedent basis.

All dependent claims are rejected to for having the same deficiencies contained in the claims they are dependent from. Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8 Claims 9-13 are rejected under 35 U.S.C. 102(b) as being anticipated by Mayfield et al. [US 6,535,962 B1] (hereinafter "Mayfield").

Per claim 9, Mayfield teaches a processor (the processing unit containing microprocessor, L2 and L3 caches; see col. 4, lines 3-23) comprising:

a cache memory to store a plurality of data (L2 and/or L3 cache, see Fig. 1 and 2);

a processor core to generate addresses corresponding to data stored within the cache memory (addresses that match cache lines in L2) ;

a plurality of buffers (cache lines in L1) from which the processor core may retrieve copies of data stored within the cache memory, the plurality of buffers being associated with a plurality of locations within the cache memory (the prefetched caches lines from L2 into L1 that match the processor addresses are used to service the processor requests instead of the cache lines in the L2 cache; see col. 2, lines 51-64 and col. 5, lines 1-14), wherein the plurality of buffers are present within the cache memory.

Per claim 10, Mayfield further teaches a selection unit to select one of the plurality of buffers from which to retrieve data (there must be a unit to select the L1 cache lines that are hit by the addresses).

Per claim 11, Mayfield further teaches aligning and signing logic to appropriately shift and apply appropriate sign information to data stored within the buffer selected by the selection unit (processors have shifters and sign-extension functional units).

Per claim 12, Mayfield further teaches a buffer control unit to detect whether an address generated by the processor core corresponds to data stored within any of the plurality of buffers, and if so, to select data within the plurality of buffers to which the address generated by the processor core corresponds (processor requests result in checking the L1 cache first for a hit, if the requested data has been prefetched or otherwise already exists in L1, the request is serviced by the L1 cache; see col. 2, lines 51-64 and col. 5, lines 1-14).

Per claim 13, Mayfield further teaches validation indicators to indicate whether data stored within the load buffers is valid (L1 cache entries have valid bits for indicate that the entries are valid for tag comparison).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 14-17 and 34-38 are rejected under 35 U.S.C 103(a) as being unpatentable over Mayfield, in further view of Patterson and Hennessy [Computer Architecture A Quantitative Approach] (hereinafter "Patterson").

Per claims 14 and 15, Mayfield does not teach the validation indicators are to indicate that data within all of buffers is invalid if the processor core has performed or will perform a write operation to a location within the cache memory to which any of the buffers corresponds. However, Mayfield teaches a multiprocessor system with shared L2 and L3 caches and distributed L1 caches (see Mayfield, Fig. 1). Patterson teaches write invalidate protocol in a multiprocessor system with distributed cache to maintain coherency (see Patterson, pages 658-666). The write invalidate protocol invalidates other copies of cache lines when a processor writes to its own copy of the cache lines to gain exclusive access and achieve cache coherency (here the other copies of cache are considered to be all of the buffers). Therefore, it would have been obvious to one ordinarily skilled in the art at the time of the applicant's invention to use the write

invalidate protocol to maintain cache coherency in Mayfield's system by invalidating other copies of cache lines when a processor writes to its own copy of the cache lines.

Per claims 16 and 17, Mayfield teaches a plurality of tag storage units to store portions of the cache memory address to which the buffers correspond (see Mayfield, Fig. 1, a cache line must have a tag portion for determination of cache hit/miss), and further teaches a comparator unit to compare contents of the tag storage unit to a portion of a cache memory address generated by the processor core (processor generated address is compared to the tag portion of the cache line to determine hit/miss).

Per claim 34, the claim is already substantially disclosed by claims 9 and 14 as set forth above.

Per claim 35, the claim is already substantially disclosed by claim 34 and 10 as set forth above.

Per claim 36, the claim is already substantially disclosed by claim 35 and 11 as set forth above.

Per claim 37, the claim is already substantially disclosed by claim 34 and 12 as set forth above.

Per claim 38, the claim is already substantially disclosed by claim 37 and 13 as set forth above.

Response to Arguments

11. Applicant's arguments with respect to claims 9-17 and 34-38 have been considered but are moot in view of the new ground(s) of rejection. The newly amendment limitations are taught by Mayfield, in further view of Patterson as set forth above.

Regarding the Applicant's argument that Mayfield does not teach the claimed feature in claim 9 which states "the plurality of buffers are present within the cache memory", the claim is rejected under 35 USC paragraph 1 as set forth above for failing to comply with the written description requirement.

Allowable Subject Matter

12. Claims 1-8 and 40-45 have been allowed.

Claim 39 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Claim 1 is allowable for citing the limitation "buffer logic to determine whether at least a portion of the first data value stored in the buffer unit corresponds to the address value based on, at least in part, detection of an overflow signal".

Claim 39 is allowable for citing the limitation "the validation indicators are to indicate that data within all of the buffers is invalid if the buffer control unit receives a clear signal from the processor core".

Claim 40 is allowable for citing the limitation "overflow logic to indicate if a corresponding buffer includes valid data based, at least in part, on an overflow signal from the adder".

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shawn Gu whose telephone number is (571) 272-0703. The examiner can normally be reached on 9am-5pm, Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon can be reached on (571) 272-4204. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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23 July 2007